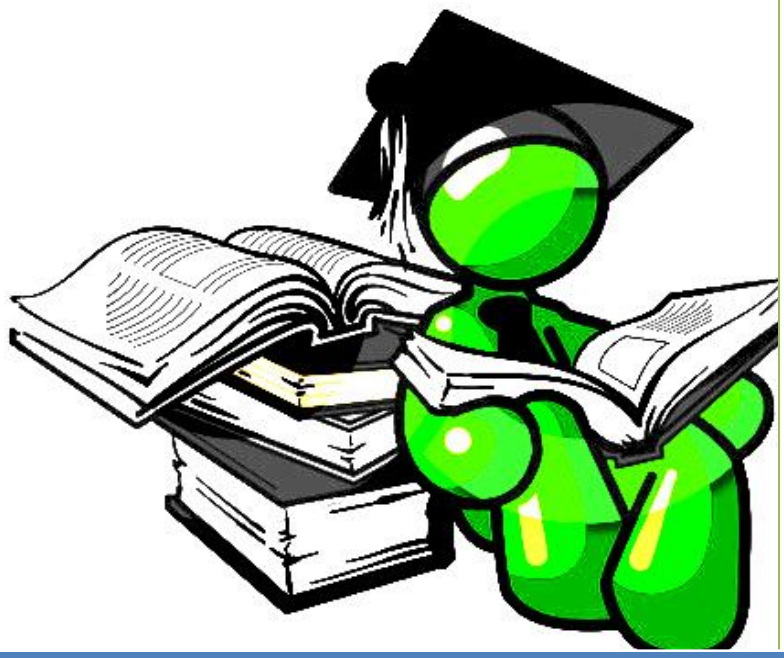
SH-2015



ACADEMIC BOOK

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
COLLEGE OF ENGINEERING
SINCERITY SACRIFICE
SYSTEM 1990
Empower The Knowledge

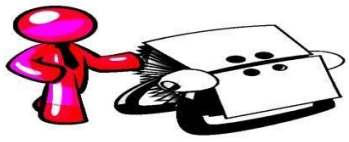
SEMESRTER VII

BE-ELECTRONICS

SH-2015

ACADEMIC BOOK

INDEX



Rules and Regulations

College Timings:
The college timing is from 8:45 AM to 4:45 PM .The students must follow the college timing.

Academic calendar and Time table:
The details of academic curriculum and activities are mentioned in the academic book. The students are required to strictly follow the class Time table and academic calendar.

Attendance:
All students are hereby informed that attendance for lectures/practical/tutorials is compulsory. Mumbai University does not allow students to appear for examination if their attendance is less than 75%.But for the good academic performance of the students, the department expects 100 % attendance in theory and practical separately.

Defaulters:
Defaulters list will be displayed monthly. The defaulter students are required to bring their parents/guardians within four days after the display of defaulters list. If students remain defaulter consistently he/she has to face the consequences as laid by the Mumbai University.

Identity card:
Student must wear ID during college hours in the campus.

Mobile Phone:
Use of cell phone is strictly prohibited in the college premises.

Examination:
As per the university norms, there will be two term test i.e Mid Term test and End Term test in the semester which is an integral part of Internal Assessment for every subject. Both the examination will be based on 40 % and 70 % of theory syllabus respectively for each subject and will be conducted as per the dates mentioned in the academic calendar. Attendance for both internal examination IS COMPULSORY .As per the university norms, no retest will be conducted under any circumstances. Separate passing heads is compulsory for internal and external examination for individual subjects. If the student fails in any of the exam he/she has to reappear in the concerned subject after the declaration of the result.

Practicals/tutorials/Assignments:
The Student should compulsory bring their rough and fair journal for the concerned subject for every practical and tutorials and get it checked regularly. Failing to do so, they will not be allowed for the practical. The Assignments for every subject should be submitted on regular basis.
The student must abide by the above mentioned rules and regulations laid down by the department for their better and brighter future.

ACADEMIC CALENDER SH-2015

COMMENCEMENT OF SEMESTER

Sr. No.	Date	Activity	Responsibility
1	June 06, 2015	Mini Project Orientation Seminar for TE	TE Project Coordinators
	June 30, 2015	Display of Timetable	Time Table Committee
2	July14, 2015	Commencement of Term Address of HODs/ faculty to the student with faculty introduction. Theory and lab period as per time table. (Small orientation lecture are to be organized on first day and course content with industry relevance to be illustrated for all classes. Rules regulations to be explained too.)	HODs / CAs and faculties Distribution of Academic Book to all students Semester wise I.III,V,VII
3	July 18, 2015	Ramzan-Id	
4	July 24, 2015	Final Mini Project Group Formation(TE)	TE Project Coordinator
5	July 24, 2015	Project approval seminar and Display of approved project :Title and Name of Guide	BE Project coordinator
6	As per department's academic Calendar	Lecture Series	As per departmental Academic Time Table
7	July 31, 2015	Project Approval Seminar (TE)	Project coordinator
9	August 06, 2015	Display of approved Mini project(TE)	TE Project Coordinator
10	August 11-14, 2015	Introduction & Initial Mini Project development (TE)	TE Project Coordinator
11	August 14, 2015	**Display of defaulter's list – I**	**Class Advisors/ HODs (Reports to be generated through MIS)**
12	August 14,2015	Fresher's Party	Student's Council & SE Students
13	August 15,2015	Independence Day	Celebrated in the college as per circular
14	August 17-21, 2015	Literature Survey	TE Project Coordinator
15	August 18,2015	Parsi New Year	
16	August 17th ,18th & 19th ,2015	Students Feedback 1	Sys Admin (Online feedback in coordination with the departments)
17	**August 24-26,2015**	**Mid Term Test**	**HODs, CAs**

18		BE Project Review – I	BE Project coordinator
19	August Last week 2015	Mini Project Review	TE Project Coordinator
20	September 1-4, 2015	Practical work of Mini Project activities	TE Project Coordinator
21	September 6,2015	Gopalkala	
22	September 7 to 11th ,2015	Parent Teachers Interaction Meeting	HODs/ CAs
23	September 8-18, 2015	Implementation of Mini Project	TE Project Coordinator
24	**September 14 , 2014**	**Display of defaulter's list – 2**	**Class Advisors/ HODs (Reports to be generated through MIS)**
25	**September 14 to 18th,2015**	On line Examination	Coordinators/ Sys Administrator / Subject Teacher
26	**September 15, 2015**	Felicitation to toppers (Engineers Day)	Principal and Student's Council
27	**September 17, 2015**	Shri Ganesh Sthapana	Principal and Student's Council
28	**September 18, 2015**	Project Review – II and Submission of softcopy of synopsis	BE Project coordinator
29	**September 21,2015**	ShriGanesh Visarjan	Principal and Student's Council
30	September 22-25, 2015	Results & Conclusion	TE Project Coordinator
31	**September 25 ,2015**	Bakari ID (ID UL ZUHA)	
32	**September 27,2015**	Anant Chaturdashi	
33	**September 28-30 , 2015**	Students Feedback 2	Sys Admin (Online feedback in coordination with departments)
34	September Last week	Mini Project review-II	TE Project Coordinator
35	**October 2,2015**	Mahatma Gandhi Jayanti	
36	**October 5-7,2015**	**End Term Test**	**HODs, CAs**
37	October 09, 2015	Final certification and submission of synopsis	BE Project coordinator
38	October 06, 2015	Project Diary & Final report submitted to guide for approval	TE Project Coordinator
39	October 10, 2015	Final submission duly approved by guide	TE Project Coordinator
40	**October 12,2015**	**Third Defaulter List**	**Class Advisors/ HODs (Reports to be generated through MIS)**
41	**October 12-23,2015**	**Remedial Classes**	Coordinators with HODs (For weaker students)

42	October 22,2015	Dasara	
43	October 19-23 ,2015	Final Certification and submission	HOD (As per University schedule)
44	October 24,2015	Moharam	
45	October 26,2015	Final defaulter list	HODs
46	October 26,2015	Term End	HODs (As per University Schedule)
47	October 26 to November 7,2015	Conduction of Oral and Practical Examinations	Faculties (As per University Schedule)
48	November 11,2015	Laxmi Pujan	
49	November 12, 2015	Balipratiprada	
50	After Term End	Vacation for faculties 1st Slot	Exam In –Charge (As per University Schedule)
51	November 25, 2015	Gurunanak Jayanti	
52	18th Nov.2015 to 19th Dec. 2015	Non Vacation Slot	(As per University schedule)
53	18th November,2015 onwards	University Theory Examination for all Semesters	Exam In-Charge (As per University schedule)
54	20th December-3rd Jan. 2016	Vacation for faculties 2nd Slot	Exam In –Charge (As per University Schedule)
55	24th December,2015	ID-E-MILAD	
56	25th December,2015	CHRISTMAS	
57	January 04,2016	Commencement of FH-2016	

Summary:

1) Total Working Weeks : 15
2) Total Working days (excluding Saturdays, Sundays & examination) : 86
3) Total Working Days for teaching : 73
4) Available Periods for teaching :

Perweek	(@)
3	42
4	56
5	70

5) Tests :

Mid Term, End Term for (FE/SE/TE/BE)	Online Test for (FE/SE/TE/BE)
02 Written test	01

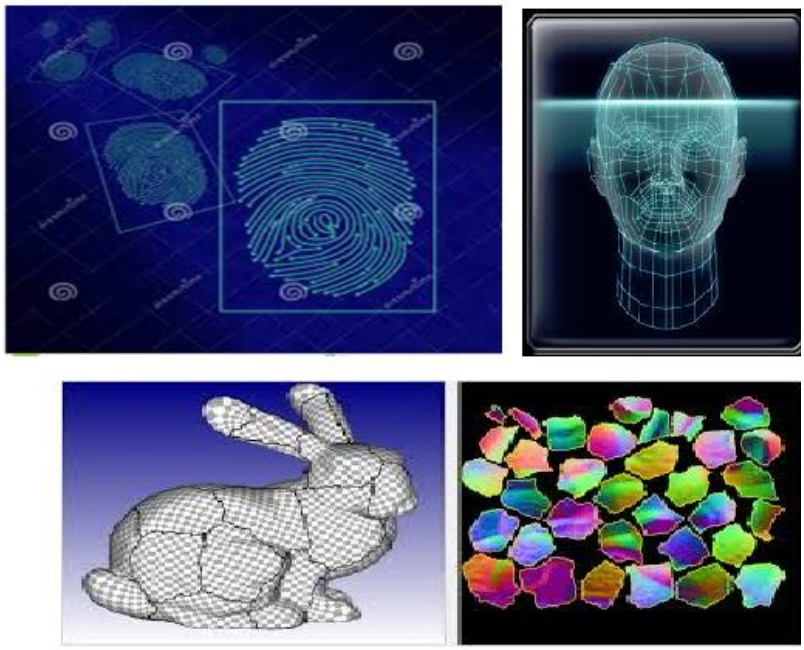
Note:

a. Attendance is compulsory from first day onwards
b. Those students who will remain absent on first day of academic semester, are compulsorily required to bring letter along with parents and meet the Principal/ HOD for permission to attend the college.
c. In case of absence (even for a day or hour), students are required to submit letters from parents at the time of attending the college.

Dr.Rajendra R.Sawant
Principal

PVPP'S

College Of Engineering



SH-2015

DIGITAL IMAGE PROCESSING

Mrs.PRITI TYAGI

PVPP COLLEGE OF ENGINEERING

(ELECTRONICS ENGINEERING)

Subject Plan

GROUP NAME: SIGNALS AND SYSTEM
COURSE TITLE : Digital Image Processing **COURSE CODE : EXC 7051** **SEM : VII(SH 2015)**
PRE-REQUISITE : EXS 401: Applied Mathematics IV EXC 504: Signals and System

COURSE OBJECTIVES :

1. To develop an overview of the field of image processing
2. To learn the fundamental concepts of Digital Image Processing.
3. To improve pictorial information for human interpretation and process scene data for storage, transmission and representation for autonomous machine perception.
4. To understand basic image enhancement and segmentation techniques.
5. To illustrate Image Transform calculations mathematically and develop fast transform algorithm
6. To learn Image Compression and Decompression Techniques

COURSE OUTCOME :

After successful completion of the course student will be able to

1. Understand the concept of Digital Image processing.
2. Explain image enhancement and Segmentation technique.
3. Understand Digital Image compression and decompression techniques
4. Perform Binary Image Processing Operations

LEARNING RESOURCES: -

RECOMMENDED BOOKS:-

1. Gonzalez & Woods, Digital Image Processing, Pearson Education, Second edition.
2. S. Jayaraman Digital Image Processing TMH (McGraw Hill) publication
3. A.K. Jain, Fundamentals of Image processing, Prentice Hall of India Publication, Third Edition

Reference Books:

1. Mc Andrew ,Introduction to Digital Image processing with Matlab, Cengage learning publication
2. Gonzalez & Woods, Digital Image Processing using MATLAB, Pearson Education
3. W. Pratt, Digital Image Processing, Wiley Publication, third edition, 2002.

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapterwise Question Bank

Evaluation :

Theory Exam	80 M
Internal assessment:-. The average marks of Mid-term test (20 M) & End-term test (20 M) will be considered as final IA marks	20 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

Topic-1 : Image Enhancement in Spatial Domain[Any two Experiments]

1. To enhance image using Histogram Equalization
2. To enhance image using Point Processing Operations
3. To enhance image using spatial filtering
4. To perform Colour Image Enhancement
5. Removal of Salt and Pepper noise

Topic-2 : Image Enhancement in Frequency Domain [Any One]

1. Find Magnitude Response and Phase Response of two images. Interchange the phase response of the two images and take Inverse Transform.
2. High Pass Filtering and Low pass Filtering

Topic-3 : Image Segmentation [Any two Experiments]

1. To find edges using LOG
2. To find Edges using Prewit/ Sobel / Robert operators.
3. To find edges using canny Edge Detection.

Topic-4 : Image Compression [Any Two Experiments]

1. To compress using Huffman coding
2. To compress DCT coefficient of Image
3. To compress Wavelet Coefficient of Image.
4. To compress Binary Image using Run Length Coding

Topic-5 : Image Transform [Any two Experiments]

1. Convolution Property of DFT
2. DWT and IDWT
3. Compute and plot DCT Basis

Topic-6 : Morphological Operations [Any One]

1. Dilation and Erosion
2. Opening and Closing Operation

SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1		**Digital Image Processing Fundamentals**	06
	1.1	**Introduction:** Background, Digital Image Representation, Fundamental Steps in Image Processing, Elements of a Digital Image Processing System	
	1.2	**Digital Image Fundamentals:** Elements of Visual Perception, A Simple Image Model, Sampling and Quantization, Some Basic Relationships between Pixels, Imagining Geometry. Image File Formats : BMP, TIFF and JPEG. Colour Models (RGB, HSI, YUV)	
2		**Image Enhancement**	08
	2.1	Spatial Domain Methods, Frequency Domain Methods, Some Simple Intensity Transformations, Histogram Processing, Image Subtraction, Image Averaging, Background	
	2.2	Smoothing Filters, Sharpening Filters, Lowpass Filtering, Highpass Filtering, Generation of Spatial Masks from Frequency Domain Specifications. Homomorphic Filtering.	
3		**Image Segmentation and Representation**	08
	3.1	Detection of Discontinuities, Edge Linking using Hough Transform, Thresholding, Region based Segmentation, Split and Merge Technique,	
	3.2	Image Representation and Description, Chain Code, Polygonal, Representation, Shape Number, Moments.	
4		**Binary Image Processing**	06
	4.1	Binary Morphological Operators, Hit-or-Miss Transformation, Boundary Extraction, Region Filling, Thinning and Thickening, Connected Component Labeling, Iterative Algorithm and Classical Algorithm	
5		**Image Transform**	12
	5.1	Introduction to the Fourier Transform, The Discrete Fourier Transform, Some Properties of the Two-Dimensional Fourier Transform Fast Fourier Transform(FFT),	
	5.2	Discrete Hadamard Transform(DHT), Fast Hadamard Transform(FHT), Discrete Cosine Transform(DCT), Discrete Wavelet Transform(DWT),	
6		**Image Compression:**	12
		Fundamentals – Coding Redundancy, Interpixel Redundancy, Psychovisual Redundancy, Fidelity Criteria.	
	6.1	Image Compression Models – The Source Encoder and Decoder, Lossless Compression Techniques : Run Length Coding, Arithmetic Coding, Huffman Coding, Differential PCM,	
	6.2	Lossy Compression Techniques: Improved Gray Scale Quantization, Vector Quantization, JPEG, MPEG-1.	
		Total	**52**

Chapterwise Plan

Subject Title: Digital Image Processing

Chapter No. : 1

Chapter Name : Digital Image Fundamentals

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Image Processing System
2	Digital Image Representation
3	Uniform and Non-uniform Sampling and Quantization
4	Basic relationship between pixels
5	Visual Perception
6	Image File formats

Objectives:

1. To define scope of Image Processing.
2. To give an idea of the state of the art in image processing by examining some of the principal areas in which it is applied.
3. To discuss principal approaches used in digital Image Processing.
4. To provide an overview of the image processing system which includes various elements such as Image acquisition, sampling, Quantization, Processing Storage and display
5. To generate digital image from sensed data.
6. Digital Image fundamentals
7. To represent image in matrix form.
8. To understand different image file formats.

Model Questions:

1. Explain the elements of digital image processing system. (10)

2. State **true** or **false** and justify :
(a) In general, fine sampling is preferred in smooth regions, while coarse sampling is preferred in regions, where grey level transitions are sharp.
(b) Quality of the picture depends on the number of pixels and the number of grey level that represent the picture.

3. Write short notes on the following :
(a) Connectivity of pixels.
(b) Image Sampling and Quantization
(c) Non uniform sampling and Quantization
(d) Spatial and Tonal Resolution
(e) Image Acquisition Methods

4. Consider the image segment shown below:

```
        3  1  2  1 (q)
        2  2  0  2
      1  2  1  1
   (p) 1  0  1  2
```

Compute the length of the shortest 4, 8, and m path between p & q.

5. Define
a. Euclidean Distance
b. City Block distance
c. Chess Board Distance
d. 4, 8. M connectivity

Chapterwise Plan

Subject Title: Digital Image Processing

Chapter No. : 2 A

Chapter Name : Image Enhancement in Spatial Domain

Approximate Time Needed : 04 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
07	Point Processing operations
08	Histogram processing
09	Histogram processing
10	Mask processing operations

Objectives:

1. To yield a better quality image for the purpose of some particular application that can be done by suppressing the noise and improve the image contrast
2. To learn Image Enhancement algorithms employed to emphasize, sharpen or smoothen image features in spatial domain for display and analysis.
3. To improve the quality of an image as perceived by a human being.
4. To discuss a number of techniques for intensity transformations and spatial filtering

Model Questions:

..State **true** or **false** and justify (4 marks each)

(a) Enhancement process does not change the information contents of the image.

(b) For digital images having salt-pepper noise, median filter is the best filter.

(c) The discrete histogram equalization technique will not, in general, yield a flat histogram.

(d) A Highpass - filtered image can be obtained in the spatial domain as
Highpass = Original - Lowpass.

(e) The principal operation of median filter is to force points with distinct intensities to be more like their neighbors.

(f) Second pass of Histogram equalization will produce same result as the first pass.

(g) The sum of the coefficients of high pass mask should be one.

2. Histogram of a digital image with eight quantization level is given below. Perform histogram equalization. Derive the transformation function and the new histogram. (10)

Grey level r	0	1	2	3	4	5	6	7
Number of pixels nr	40	60	80	120	140	160	180	220

3. A digital image with eight quantization levels has the following histogram perform histogram equalization and derive transformation function. Give new equalized histogram.

Grey level r	0	1	2	3	4	5	6	7
No. of Pixels with grey level n_r	120	160	200	150	80	80	100	110

4. Explain briefly the following operations to digital images along with one application for each : (10)
(i) Median filter. (ii) Image subtraction. (iii) Contrast stretching. (iv) Bit plane slicing.
(v) Thresholding.

5. Perform zooming operation using linear interpolation as well as replication, on following image. State which method performs generally better. (4)

40	60	55	50
45	62	48	55
20	24	27	34
07	06	40	45

6. Give following masks of size 3×3 and explain their usefulness in image processing (any **four**) : (8)
(i) Sobel (ii) Roberts (iii) Low-pass filter (iv) Prewitt

7. Suppose that a digital image is subjected to histogram equilization. Show that second pass of histogram equilization will produce exactly the same result as first pass. (10)

8. (a) Apply the following Image Enhancement techniques on the given Image. (10)

(i) Digital Negative (ii) Bit Plane Slicing (iii) Thresholding

Image

2	1	3	4	5
7	4	2	0	1
3	5	1	4	6
0	4	0	2	3
2	1	6	1	4

9. Apply Low Pass and High Pass Spatial Mask on the following image matrix

$$F = \begin{bmatrix} 5 & 4 & 7 & 1 & 2 \\ 6 & 2 & 3 & 4 & 1 \\ 3 & 5 & 6 & 8 & 2 \\ 4 & 3 & 7 & 1 & 8 \end{bmatrix}$$

10. Apply Low Pass and High Pass Spatial Mask on the following image matrix
Prove that Highpass=Original – Lowpass. Assume virtual rows and columns

30	31	32
33	120	30
32	32	31

11.

Plot the histogram for the following image. Equalize the histogram and then plot the equalized histogram and the image corresponding to the equalized histogram. The 4 × 5 image is represented by 3 bits/pixel.

1	3	3	3	2
3	2	3	1	2
5	1	1	1	4
5	6	6	7	0

12

12 Differentiate between point processing and mask processing operations. Classify the following operations into point processing and mask processing operations

(i) Gray Level slicing
(ii) Median filtering
(iii) High pass filtering
(iv) Edge detection with sobel operator
(v) Dynamic range compression
(vi) Thresholding

Draw the transfer characteristics of any two point processing operations.

Chapterwise Plan

Subject Title: Digital Signal Processing and Processors

Chapter No. : 2B

Chapter Name : Image Enhancement in Frequency Domain

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
11	2D -Fourier Transform
12	2D-DFT
13	Properties of 2D DFT
14	FFT
15	LPF, HPF (Ideal, Butterworth, Gaussian)
16	High Boost filtering, Homomorphic filtering

Objectives:

1. To yield a better quality image for the purpose of some particular application that can be done by suppressing the noise and improve the image contrast
2. To learn Image Enhancement algorithms employed to emphasize, sharpen or smoothen image features in frequency domain for display and analysis.
3. To establish a foundation for the fourier Transform and how it is used in basic image filtering
4. To implement Fourier transform in the context of Image processing
5. Formulation of filtering in the frequency domain.
6. Homomorphic filtering

Model Questions:

1. Write short notes on the following :
   (a) Homomorphic filtering.
   (b) Discrete Fourier Transform
2. Prove that if an image f(m,n), $0 \le m \le M-1$ and $0 \le n \le N-1$ is multiplied by the checkerboard pattern $(-1)^{m+n}$, Then its DFT is centered at (M/2,N/2)
3. List any two properties of 2D DFT and prove any one of them.
4. Explain with block diagram basic steps for filtering in frequency domain.
5. What are the steps required to perform filtering in the frequency domain. Also explain the Butterworth Low Pass Filter.
6. Explain separability and Translation property of DFT for an image.
7. Show that 2D-DFT of an image can be computed by row & column passes with 1D DFT algorithm.

Chapterwise Plan

Subject Title: Digital Image Processing

Chapter No. : 3

Chapter Name : Image Segmentation and Image Representation

Approximate Time Needed : 09 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
17	Image Segmentation Based on Discontinuity
18	Edge Detection
19	Hough Transform
20	Graph – Theoretic Techniques
21	Thresholding
22	Region based Segmentation
23	Region based Segmentation
24	Image Representation
25	Chain Code

Objectives:

1. Image Segmentation is aa essential preliminary step in most automatic pictorial pattern recognition and scene analysis applications.
2. To subdivide an image into its constituent regions or objects.
3. To extract various features of the image which can be merged or split in order to build objects of interest on which analysis and interpretation can be performed
4. To analyze the content of the image and extract important features from image data.
5. Learn various thresholding techniques.
6. Learn different shape representation techniques

Model Questions:

1. State **true** or **false** and justify :
   (a) Segmentation algorithms for monochrome images generally are based on two basic properties of grey level values.
   (b) Poorly illuminated images can be easily segmented.
   (c) Laplacian is not a good edge detector.

2 (a) Describe edge detection via graph-theoretic technique. (5)
(b) Describe all possible masks for line detection. (5)
(c) Assume that the edge in the grey-level image starts in the first column and ends in the last column. Find the cost of all possible edges and sketch them. Find the edge corresponding to minimum cost path. (10)

2	1	0
1	1	7
6	8	2

(a) Explain Segmentation based on discontinuity and Segmentation based on similarities. 8

(b) Design compare gradient operators of size 3 × 3 to measure gradients of edges oriented in eight directions. 8

E, NE, N, NW, W, SW, S and SE.

Give the form of these eight operators using coefficients valued 0, 1, or −1 also specify the gradient direction of each mark.

3 (c) Explain Region oriented Segmentation. 4

(a) Assuming that the edge starts on the first column and ends in the last column for the following grey level image. 15

Sketch all possible paths and determine the edge corresponding to minimum cost path.

k \ j	0	1	2
0	2	1	0
1	1	1	7
2	6	8	2

4.

5. Explain the method of segmentation of images by
   (i) Region Growing
   (ii) Region Splitting
   (iii) Region Split and Merge

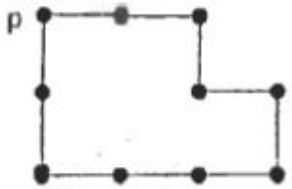
6. Obtain the 4 Directional Chain code for the image shown below

7. Write short notes on
   a. Polygonal Approximation and Signatures.
   b. Region Based Segmentation

c. Fourier Descriptor
d. Hough Transform
e. Point Detection
f. Chain Code

8.

Obtain the 4 Directional Chain code for the image shown below. Find first Difference and circular first difference.



Chapterwise Plan

Subject Title: Digital Image Processing

Chapter No. : 4

Chapter Name : Image Compression

Approximate Time Needed : 12 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
26	Introduction
27	Data Redundancy
28	Image Compression Model
29	Lossless Compression (Variable Length Coding)
30	Lossless Compression (LZW, Bit Plane Coding)
31	Arithmetic Coding
32	Arithmetic Coding
33	Fidelity Criteria
34	Differential PCM
35	IGS Coding
36	Vector quantization
37	JPEG, MPEG I

Objectives:

The student will learn

1. Compact Image representation
2. To reduce the amount of data required to represent an image
3. Techniques to compress amount of data needed to represent information.
4. To find statistical properties of the image to design an appropriate compression transformation of the image.
5. Image compression standards

Model Questions:

1. State **true** or **false** and justify :
(a) Variable length coding procedures can be used to compress a histogram equalized image with 2^n grey levels.
(b) All image compression techniques are invertible.
(c) Run length coding always gives data compression.
(d) Runlength coding is loss-less coding but may not give data compression always.
(e) In transform based image compression, DCT is widely used as compared to other Transforms.

2. (a) Generate Huffman code for the given source. Calculate entropy of the source, average length of the code and the compression ratio achieved :
Symbol

Symbol	a1	a2	a3	a4	a5	a6	a7	a8
Probability	0.06	0.02	0.3	0.5	0.04	0.01	0.03	0.04

(b) Consider an 8-pixel line grey-scale data, {12, 12, 13, 13, 10, 13, 57, 54}, which has been uniformly quantized with 8-bit accuracy. Construct its 3-bit IGS code. State and explain in brief the type of redundancy which is exploited here to achieve compression.
3. Write short notes on the following :
(a) Fidelity criteria. (b) Transform Coding

4 For a given source A = {a1, a2, a3, a4} the following codes were developed. Check for each of them whether it is uniquely decodable or not. Also state which one is the most optimum compared to others and why ? (8)

Symbols	Probability	Code 1	Code 2	Code 3
a_1	0.5	0	0	0
a_2	0.25	1	10	01
a_3	0.125	00	110	011
a_4	0.125	11	111	0111

5.

(a) Explain basic data rudendancies. Describe basic compression model used for image compression. 8

(b) Classify with reasons, the following data compression techniques into lossy and lossless schemes : (i) Run Length Coding (ii) DCT Compression. 8

(c) How many Unique Huffman Codes are there for three symbol source ? Construct these codes. 4

6.

What are the different types of redundancies that can be present in a digital image and state which method can be used to remove/reduce them ? 8

7. Obtain Huffman Code for the word "COMMITTEE"

8. Draw and explain Block diagram of JPEG Encoder & Decoder. (10 marks)
9. Mention different steps employed in coding of images using vector quantization
10. Encode the statement "I LOVE IMAGE PROCESSING " using the Arithmetic Coding Procedure

Chapterwise Plan

Subject Title: Digital Image Processing

Chapter No. : 5

Chapter Name : Image Transform

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
38	Matrix Theory
39	Discrete Cosine Transform
40	Discrete Cosine Transform
41	Discrete Hadamard Transform
42	Fast Hadamard Transform
43	Fast Hadamard Transform
44	Discrete Wavelet Transform
45	Discrete Wavelet Transform

Objectives:

1. To learn Efficient representation of visual information
2. Ability to capture significant information of an image in a small description.
3. To study 1D and 2D unitary transforms and its properties.
4. To gain knowledge of several unitary transforms like DFT, DCT, Hadamard and Wavelet Transform and its implementation on images.

Model Questions:

1. Explain any two properties of 2-dimensional Fourier transform. (4) If f = [1 0 2 3 4 1 3 1]t ; find its Hadamard transform. (5)

2. (a) Explain the property of Hadamard Transform, also find the Hadamard Transform of $f(x) = \{1, 2, 2, 1\}^t$ 8

(b) Three column vectors are given below :- 8

$$x_1 = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}, \quad x_2 = \begin{bmatrix} -2 \\ 1 \\ 1 \end{bmatrix}, \quad x_3 = \begin{bmatrix} 0 \\ -1 \\ 1 \end{bmatrix}$$

show that they are orthogonal, also generate all Possible Pattern.

(c) Explain the following Property of Image Transform 4

(i) Symmetrical (ii) Orthonormal.

1. Compute DFT and DCT of the following Image

1	3	4	5
3	2	6	4
4	6	2	3
5	4	3	1

2. Show that 2D-DCT can be computed by row and column passes with 1D-DCT algorithm
3.
4. For 2x2 transform A and the image U, Compute Transformed image V and the basis image

$$A = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}, \quad U = \begin{bmatrix} 1 & 2 \\ 3 & 4 \end{bmatrix}$$

5. Justify/ Contradict the following Statements
   a. If kernel of an image transform is separable and symmetric, the transform can be expressed in matrix form.
   b. Walsh Transform is nothing but sequency ordered Hadamard matrix

6. Let $A = \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$, $B = \begin{bmatrix} 1 & 2 \\ 3 & 4 \end{bmatrix}$. Find Kronecker Products $A \circledast B$ and $B \circledast A$ Comment on your result.

7. Write the expression of DFT. State and explain the properties of 2D-DFT.

8. Write short note on 2D wavelet Transform Filter Bank.

9. For the following 4 x 4 image, determine its forward and inverse transforms and compare the inverse transform with the digitized image. $\begin{bmatrix} 2 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 2 & 1 & 2 & 3 \end{bmatrix}$

   (i) DFT (ii) DCT

Chapterwise Plan

Subject Title: Digital Image Processing

Chapter No. : 6

Chapter Name : Binary Image Processing

Approximate Time Needed : 07 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
46	Binary Morphological Operators
47	Hit-or-Miss Transformation,
48	Boundary Extraction, Region Filling
49	Thinning and Thickening
50	Connected Component Labeling
51	Iterative Algorithm and Classical Algorithm
52	Iterative Algorithm and Classical Algorithm

Objectives:

This chapter gives overview of different operations involved in Binary Image Processing.
The objective is to make the students familiar with the following concepts

1. Basic idea of mathematical morphology
2. Binary morphological operations like thinning, thickening, hit or miss transform etc.

Model Questions:

1. Explain the following operations
   1. Erosion
   2. Dilation
   3. Closing
   4. Opening

2. Explain HIT or MISS Transformation
3. Explain the importance of boundary extraction. Generate an algorithm to perform the same.
4. Explain the following transformation in detail
   1. Thinning
   2. Thickening
   3. Skeletonization
   4. Pruning

ASSIGNMENT (CASE STUDY)

DATE OF SUBMISSION : 30th September 2015

Group No.	*Case Study*
E1	*Digital Watermarking*
E2	*Face Recognition*
E3	*Finger print Recognition*
E4	*Signature Recognition*
E5	*Vehicle number plate detection and recognition*
E6	*Object Detection using Correlation principle*
E7	*Person Tracking using DWT*
E8	*Handwritten Character recognition*
E9	*Printed Character Recognition*
E10	*Content based image retrieval*
E11	*Text Compression*
E12	*Image Compression Standards*
E13	*Image processing techniques for mobile applications*
E14	*Image Acquisition*
E15	*Satellite Images*
E16	*Change Detection*
E17	*Thresholding*
E18	*Adaptive Thresholding*
E19	*Medical Image Processing*
E20	*Satellite Image Processing*

FORMAT FOR CASE STUDY

Abstract :
Introduction :
Literature Survey :
Conclusion :

B.E. ETRX VII (R)
DIPD

21/5/15

QP Code : 8469

Duration 3 Hours **Maximum marks 100**

Instructions :

1. Question No.1 is compulsory.
2. Out of the remaining questions attempt any four.
3. Figures in the bracket indicate maximum marks.

Q 1. Answer the following:

a) What do you mean by zero memory operations? [05]

b) Differentiate between 8 connectivity and m connectivity. [05]

c) What is truncated Huffman code? [05]

d) Justify the statement: " Laplacian filter is a high pass filter." [05]

Q 2.

a) Explain the following enhancement operations and draw the graph of transformation function: [10]

i) Dynamic range compression ii) Gray level slicing

b) Perform histogram equalization on the following image histogram and plot original and equalized histograms. [10]

Gray Level	0	1	2	3	4	5	6	7
Number of pixels	550	300	0	0	0	200	325	225

Q 3.

a) Explain in detail the types of data redundancies seen in digital images [10]

b) Explain the method of edge linking using Hough Transform. [10]

Q 4.

a) Calculate the 2DDFT and Hadamard transform of the image segment shown below using matrix multiplication method. [08]

$$f(x,y) = \begin{matrix} 0 & 0 & 1 & 4 \\ 1 & 1 & 1 & 4 \\ 1 & 0 & 1 & 0 \\ 0 & 2 & 0 & 2 \end{matrix}$$

b) Explain the importance of kernel separability property of 2DDFT in implementing 2DFFT. [06]

c) Differentiate between spatial and tonal resolution. [06]

Q 5.

a) Explain why it is difficult to threshold images with poor illumination. [10]

b) With the help of a neat block diagram, explain the working of a homomorphic filter. [10]

Q 6.

a) What are Fourier Descriptors? Explain how a two dimensional boundary is represented using Fourier Descriptors. [10]

b) Explain how Huffman code removes coding redundancy. [10]

Q 7. Write short notes on any **four** of the following: [20]

a) Moments b) Wavelet transform

c) Digital water marking d) Biometric authentication

e) Motion based segmentation

RJ-Con. 10025-15.

Elective II Elective ... 27/11/2014

BE
Sem VII

Digital Image Processing System

QP Code :15360

(3 Hours) **[Total Marks : 100**

N.B : (1) Question No. **1** is **compulsory**.
(2) Out of the remaining questions attempt any **four**.
(3) **Figures** in the **right** indicate maximum **marks**.

1. Answer any **four** :
   (a) Differentiate between spatial and tonal resolutions. **5**
   (b) Why is the sum of coefficients of a high pass filter mask zero? **5**
   (c) Compare Huffman coding and arithmetic coding; **5**
   (d) Give 3x3 masks for Laplacian filter, horizontal, vertical, +45° and -45° line detectors. **5**
   (e) Explain dilation and erosion in brief. **5**

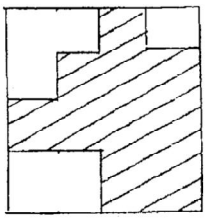
2. (a) Explain the following enhancement operations and draw the graph of transformation function : **10**
   (i) Clipping, (ii) Bit plain slicing
   (b) Perform histogram equalization on the following image histogram and plot original and equalized histograms. **10**

Gray Level	0	1	2	3	4	5	6	7
Number of pixels	200	300	500	350	250	0	0	0

3. (a) A source emits 6 symbols with the following probabilities : **10**

Symbol	A	B	C	D	E	F
Probability	0.1	0.2	0.05	0.05	0.35	0.25

   Construct the Huffman code. Calculate the average code word length and coding efficiency.
   (b) Perform region splitting and merging on the image segment shown below. Draw the quad tree. Briefly explain the method used. **10**



4. (a) Calculate the Hadamard transform of the image segment. 5

$$f(x,y) = \begin{bmatrix} 2 & 3 & 1 & 4 \\ 2 & 1 & 1 & 4 \\ 1 & 3 & 4 & 4 \\ 3 & 3 & 2 & 2 \end{bmatrix}$$

(b) State and prove any two properties of 2DDFT. 5

(c) Obtain the 16 basis images of Hadamard transform. 10

5. (a) Given the 8 x 8 image segment, perform erosion using the structuring element shown: 10

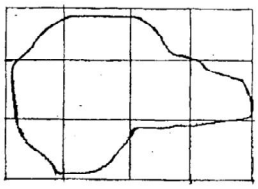
1	0	0	0	0	0	0	1
1	1	0	0	0	0	1	1
1	1	1	0	0	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	0	0	1	1	1
1	1	0	0	0	0	1	1
1	0	0	0	0	0	0	1

Structuringelement :

1	1
1	1

(b) With the help of a neat block diagram, explain the working of the homomorphic filter. 10

6. (a) What are chain codes? Obtain 4 connected and 8 connected chain codes for the boundary shown below: 10



(b) Explain in detail different types of data redundancies present in the digital images 10

7. Write short notes on any four of the following: 20
   (a) Opening and closing
   (b) Color models
   (c) Finger print recognition
   (d) Digital water marking
   (e) Handwritten character recognition.

Digital Image Processing Design.
Sem VII ETRX 30/11/13

14-11-13-DTP-P-14-AK-20

Con. 8482-13. **LJ-13990**

(Revised Course)

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions from the remaining **six** questions.
(3) Assume **suitable** data if **needed**.

1. Justify any **four** of the following statements :- **20**
   (a) Reduction in spatial resolution results in checker board degradation.
   (b) Huffman coding is a lossless compression technique.
   (c) Butterworth lowpass filter is preferred to ideal lowpass filter.
   (d) It is difficult to segment poorly illuminated images.
   (e) Dynamic range compression is used in displaying the Fourier transform of an image.

2. (a) The gray level distribution of an image is shown in the table below. Perform histogram equalization and plot the original and equalized histograms. **10**

Gray level	0	1	2	3	4	5	6	7
Frequency of occurrence	0	50	100	200	400	200	50	0

   (b) With the help of block diagram, explain the working of a Homomorphic filter. **10**

3. (a) A 5x5 image segment is shown below. Perform bitplane slicing and lowpass filtering on the same :- **10**

6	7	6	6	7
0	0	0	1	2
1	1	1	2	3
4	5	5	4	2
6	6	6	7	7

   (b) With the help of suitable examples, explain the following morphological operations :- **10**
   (i) Dilation
   (ii) Erosion.

4. (a) What are the different types of data redundancies found in digital images ? Explain in detail. **10**

[TURN OVER

14-11-13-DTP-Pvt-AK-21

Con. 8482-LJ-13990-13. 2

(b) A source emits six symbols with probabilites as shown in the table below. Construct the Huffman code and calculate the coding efficiency. **10**

Symbol	a_1	a_2	a_3	a_4	a_5	a_6
Probability	0.05	0.25	0.05	0.15	0.2	0.3

5. (a) Obtain the 2DDFT of the image segment shown below using any one fast algorithm. **10**

$$f(x,y)=\begin{bmatrix}0 & 0 & 1 & 1\\ 1 & 2 & 0 & 0\\ 1 & 0 & 1 & 1\\ 2 & 0 & 1 & 0\end{bmatrix}$$

(b) What is Segmentation ? With the help of examples, explain segmentation based on similarity. **10**

6. (a) Explain the following with examples :- **10**
   (i) Signature
   (ii) Fourier Descriptor.
   (b) State and prove periodicity and translation properties of 2DDFT. Write the transformation matrices for Hadamard and Fourier transforms for N = 4. **10**

7. Write short notes on any **four** :- **20**
   (a) Isopreference cuvers
   (b) Hough transform
   (c) Digital Water marking
   (d) Chain codes
   (e) Biometric Authentication.

PVPP'S
College Of Engineering

DEPARTMENT OF
ELECTRONICS ENGINEERING

BE-Electronics - Sem - VII (REV COURSE) Elective-I
Digital Image Processing Design
17/12/12

wa-Con-2012

Con. 10909–12. **(REVISED COURSE)** **KR–1863**

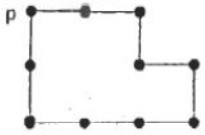
(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. 1 is **compulsory**.
(2) Assume **suitable** data wherever **necessary**.
(3) Attempt any **four** questions from remaining questions.

1	State true or false and justify (Any Four): (a) Poorly illuminated images can be easily segmented. (b) All Image Compression techniques are invertible. (c) Chain Codes can be made invariant to translation and rotation. (d) The principal operation of median filter is to force points with distinct intensities to be more like their neighbors. (e) Quality of the picture depends on the number of pixels and the number of gray level that represent the picture.	20
2 (a)	An image represented by 8 bit/pixel has following gray level distribution. Perform histogram equalization and give new distribution of gray level.	10
(b)	Explain Segmentation based on discontinuity and similarity	10
3 (a)	Obtain Huffman Code for the word "COMMITTEE"	10
(b)	Explain Homomorphic filtering.	10
4(a)	What are the different types of redundancies in an image? Explain how they can be reduced / eliminated.	10
(b)	List any two properties of 2D DFT and prove any one of them.	10
5 (a)	Apply the following Image Enhancement techniques on the given Image. (i) Digital Negative (ii) Bit Plane Slicing (iii) Thresholding	10
(b)	Obtain the 4 Directional Chain code for the image shown below. Find first Difference and circular first difference.	10
6 (a)	For 2x2 transform A and the image U, Compute Transformed image V and the basis image $A = \frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & 1\end{bmatrix}$, $U = \begin{bmatrix}1 & 2\\ 3 & 4\end{bmatrix}$	10
(b)	Give following masks of size 3×3 and explain their usefulness in image Processing. (i) Sobel (ii) Roberts (iii) Low-pass filter (iv) Prewitt (v) Laplacian	10
7	Write short notes (**Any Four**) (i) Dilation and erosion (ii) Image Sampling (iii) JPEG (iv) Connectivity of pixels (v) Filtering in Frequency domain	20

Gray Level	0	1	2	3	4	5	6	7
Number of pixels	128	75	280	416	635	1058	820	684

2	1	3	7	4
4	5	2	0	1
3	5	1	4	6
0	4	0	2	3
2	1	6	1	4



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DEPARTMENT OF
ELECTRONICS ENGINEERING

22/12/2011 BE ETRX Sem-VII (Rev)
Digital Image Processing
Design

PR-Oct. (1) 178
Con.6842-11.

MP-5593

(REVISED COURSE)

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. 1 is **compulsory.**
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Assume any suitable** data if **necessary.**

1. State whether the following statements are **true** or **false.** Justify your answer– 20
   (a) Low pass filter is smoothening filter.
   (b) Huffman coding is a lossless data compression technique.
   (c) Median filter is used to remove salt and pepper noise.
   (d) Quality of picture does not depend on the number of pixels and gray levels that represent the image.

2. (a) An image segment of 4 × 4 size with 3 bits per pixel is shown below. Perform the following operations– 10
   (i) Image Negative
   (ii) Bit plane slicing–

0	7	1	2
2	5	3	2
1	4	5	6
3	2	5	2

   (b) What do you understand by sampling and quantization with respect to digital image processing ? How will you convert an analog image into a digital image. 10

3. (a) Discuss advantages of homomorphic filtering. Also explain the steps of homomorphic filtering with the help of a neat block diagram. 10
   (b) Name different types of image segmentation techniques. Explain the splitting and merging technique with the help of an example. 10

4. (a) Compare between contract stretching and histogram equalization. 10
   (b) What do you understand by Hadamard Transform ? Write a 4 × 4 Hadamard Matrix. Discuss application of Hadamard Transform.

5. (a) Name and explain different types of redundancies in digital image. 10
   (b) Explain image compression model with the help of a neat block diagram. 10

6. (a) How will you detect following in a digital image ? 10
   (i) Point
   (ii) Line
   (iii) Edge.
   (b) Define two dimensional Discrete Fourier Transform (2D – DFT). Explain the properties of 2D – DFT in detail. 10

7. Write short notes on the following :– 20
   (a) Biometric Authentication
   (b) Dilation and Erosion
   (c) Digital Watermarking
   (d) Lossless Compression.

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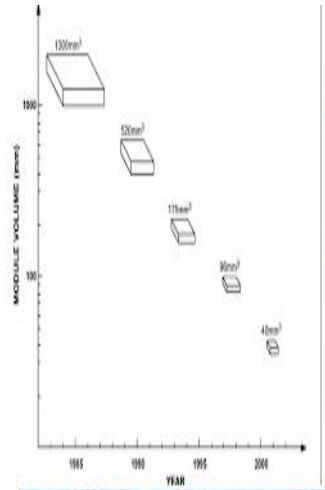
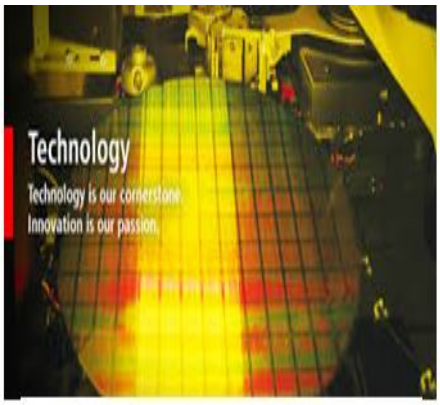
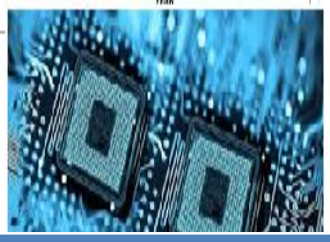
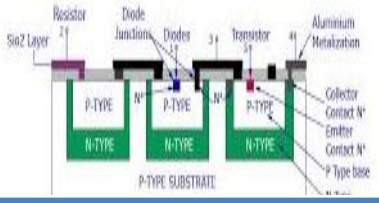




Basic Monolithic IC Cross-Sectional View





SH 2015

IC TECHNOLOGY

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
COLLEGE OF ENGINEERING
SINCERITY
SACRIFICE
SYSTEM
1990
Empower The Knowledge

Mrs.Deepali H. Bhosale

Subject Plan

GROUP NAME : VLSI
COURSE TITLE : IC Technology **COURSE CODE : EXC 702** **SEM : VII (SH 2015)**
PRE-REQUISITE :Digital Circuit Design, DLIC, Basic VLSI Design

RATIONALE

An integrated circuit or monolithic integrated circuit (also referred to as an IC, a chip, or a microchip) is a set of electronic circuits on one small plate ("chip") of semiconductor material, normally silicon. This can be made much smaller than a discrete circuit made from independent electronic components. ICs can be made very compact, having up to several billion transistors and other electronic components in an area the size of a fingernail. The width of each conducting line in a circuit can be made smaller and smaller as the technology advances; in 2008 it dropped below 100 nanometers, and has now been reduced to tens of nanometers. Integrated circuits are used in virtually all electronic equipment today and have revolutionized the world of electronics. Computers, mobile phones, and other digital home appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of integrated circuits. Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at a time. Furthermore, packaged ICs use much less material than discrete circuits.

OBJECTIVES :

5. Become familiar with different crystal growth technique
6. Understand CMOS fabrication Flow
7. To teach fundamentals of fabrication of VLSI devices and circuits
8. Provide knowledge about packaging and testing of Integrated circuits
9. Understand advanced semiconductor technologies
10. To disseminate knowledge about novel VLSI devices

OUTCOME :

1. Understand the physics of crystals and different crystal growth techniques.
2. demonstrate a clear understanding of CMOS fabrication flow and technology scaling
3. demonstrate a clear understanding of various MOS fabrication processes, semiconductor measurements, packaging, testing and advanced semiconductor technologies
4. discuss physical mechanism in novel devices
5. verify processes and device characteristics via simulations

LEARNING RESOURCES: -

RECOMMENDED BOOKS: -

1. James D. Plummer, Michael D. Deal and Peter B. Griffin, "*Silicon VLSI Technology*", Pearson, Indian Edition.
2. Stephen A. Campbell, "*The Science and Engineering of Microelectronic Fabrication"*, Oxford University Press, 2nd Edition.
3. Sorab K. Gandhi, "*VLSI Fabrication Principles*", Wiley, Student Edition.
4. G. S. May and S. M. Sze, "*Fundamentals of Semiconductor Fabrication*", Wiley, First Edition.
5. Kerry Bernstein and N. J. Rohrer, "*SOI Circuit Design Concepts"*, Kluwer Academic Publishers, 1st edition.
6. Jean-Pierre Colinge, "*FinFETs and Other Multigate Transistors"*, Springer, 1st edition
7. M. S. Tyagi, "*Introduction to Semiconductor Materials and Devices*", John Wiley and Sons, 1st edition.
8. James E. Morris and Krzysztol Iniewski, "*Nanoelectronic Device Applications Handbook*", CRC Press
9. Glenn R. Blackwell, "*The electronic packaging*", CRC Press
10. Michael L. Bushnell and Vishwani D. Agrawal, "*Essentials of Electronic Testing for digital, memory and mixed-signal VLSI circuits*", Springer

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapter wise Question Bank

Evaluation :

Theory Exam	80 M
Internal assessment:-. The average marks of Mid-term test (20 M) & End-term test (20 M) will be considered as final IA marks	20 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

At least 8 experiments based on the entire syllabus

Expt. No.	Name of the Experiments
1	Draw and simulate layout for the CMOS inverter.
2	Draw and simulate layout for the CMOS NAND and CMOS NOR circuits.
3	Draw and simulate layout for the given equation
4	Draw and simulate layout for SR latch D flip Flop circuits
5	Draw and simulate layout for 6T SRAM cell.
6	Simulate oxidation process with Deal-Grove model for different conditions (e.g. oxidation type, orientation, time, temperature, thickness etc.) and comment on the results obtained.
7	Simulate MOS capacitor (Classical Simulation) for single gate device for a typical value of fixed charge density and interface trap charge density in gate insulator. Do the AC analysis and comment on the results obtained.
8	Simulate n type and p type MOSFETs (bulk, SOI and Double Gate) to obtain family of I D-VG and ID- VD characteristics. Compare the results obtained.
9	Simulate Carbon Nanotube MOSFET for different conditions (e.g. gate/drain voltage sweep, threshold voltage etc.) and comment on the results obtained.
10	Simulate FinFET to plot energy band diagram and IV characteristics for different values of gate and drain bias. Comment on the results obtained.

Chapterwise Plan

Subject Title: IC Technology

Chapter No. : 1

Chapter Name : Environment and Crystal Growth for VLSI Technology

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Introduction
2	Semiconductor technology trend
3	Clean rooms
4	Wafer cleaning
5	Phase diagram and solid solubility
6	Crystal structure, Crystal defects, Czochralski growth
7	Bridgman growth of GaAs, Float Zone growth
8	Wafer Preparation and specifications

Objectives:

1. To teach Physics of crystals and different crystal growth techniques
2. Learn the need of wafer cleaning

Model Questions:

1. Describe the RCA cleaning process
2. Describe SC1 and SC2 cleaning process
3. Describe the different methods adopted for reducing the contamination in IC fabrication process
4. Explain the significance of phase diagram and solid solubility in IC fabrication with suitable examples.
5. Discuss different types of crystal defects in semiconductor?
6. With neat diagram explain the crystal growth using CZ method
7. With neat diagram explain the Float Zone technique of crystal growth

Chapterwise Plan

Subject Title: IC Technology

Chapter No. : 2

Chapter Name : Fabrication Processes Part 1

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
9	Deposition: Evaporation
10	Sputtering and Chemical Vapor Deposition
11	Epitaxy: Molecular Beam Epitaxy, Vapor Phase Epitaxy, Liquid Phase Epitaxy
12	Silicon Oxidation: Thermal oxidation process, Kinetics of growth
13	Properties of Silicon Dioxide, Oxide Quality, high κ and low κ dielectrics
14	Diffusion: Nature of diffusion, Diffusion in a concentration gradient
15	diffusion equation, impurity behavior, diffusion systems
16	Problems in diffusion, evaluation of diffused layers
17	Ion Implantation: Penetration range, ion implantation systems
18	Process considerations, implantation damage and annealing

Objectives:

1. Understand different techniques for Deposition, Epitaxy, Oxidation
2. Understand CMOS fabrication Flow

Model Questions:

1. Describe different reactors used for vapor phase epitaxy process
2. How evaluation of the following parameters are done for epitaxial layer:
    a. Sheet Resistance
    b. Layer Thickness
    c. Mobility and Carrier Concentration
    d. Impurity
3. Explain MBE process and list its advantages
4. Develop the equations to describe the oxidation process (Deal-Grove model)
5. Describe dopant redistribution during oxidation
6. What are linear and parabolic regimes of oxidation?
7. Describe the furnaces used for oxidation
8. What are the reactions of dry oxidation and wet oxidation? Differentiate between these two methods.
9. Differentiate between high κ and low κ dielectrics
10. Explain different types of oxide charges
11. Write the equations and boundary conditions for
    a. Constant source diffusion
    b. Limited source diffusion
12. Write the mathematical equation describing the dopant profile for
    a. Constant source diffusion
    b. Limited source diffusion
13. Describe the problems that arise due to dopant redistribution
14. What is lateral diffusion?
15. What is gettering?
16. Solve the differential equation for constant source diffusion
17. Describe the diffusion process, including the equipment used

Chapterwise Plan

Subject Title: IC Technology

Chapter No. : 3

Chapter Name : Fabrication Processes Part 2

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
19	Etching: Wet chemical etching, dry physical etching, dry chemical etching
20	reactive ion etching, ion beam techniques
21	**Lithography:** Photoreactive materials, Pattern generation and mask making, pattern transfer
22	Electron beam, Ion beam and X-ray lithography
23	**Device Isolation, Contacts and Metallization:** Junction and oxide isolation
24	LOCOS, trench isolation, Schottky contacts, Ohmic contacts
25	Metallization and Packaging
26	**CMOS Process Flow:** N well, P-well and Twin tub
27	Design rules, Layout of MOS based circuits
28	Layout Example. Buried and Butting Contact

Objectives:

1. Understand various CMOS fabrication processes
2. To teach fundamentals of fabrication of VLSI devices and circuits

Model Questions:

1. Draw the device cross sections for the important steps in fabrication of PMOS transistor
2. Draw the device cross sections for the important steps in n-well CMOS process
3. Draw the device cross sections for the important steps in p-well CMOS process
4. Draw the device cross sections for the important steps in twin tub CMOS process
5. Draw layout for the CMOS inverter
6. Draw layout for the 6T SRAM cell
7. Draw layout for two input XOR gate
8. Draw layout for two input NAND gate
9. Draw layout for two input NOR gate
10. Darw layout for 1T DRAM cell
11. What are isotropic and an-isotropic etching?
12. Give examples of reactions involved in dry etching
13. Describe plasma etching process with schematics
14. What is loading effect in etching
15. Describe Reactive Ion Etching (RIE) process
16. Describe the ion beam technique used for etching
17. Describe the basic PVD process, with schematics
18. Describe the RF sputtering process, with schematics
19. Describe the mask making process
20. Describe the lithographic process in detail
21. Explain the difference between contact, proximity and projection printing
22. Discuss electron beam lithography in detail
23. Differentiate between positive and negative photoresist
24. Describe the following methods of isolation in integrated circuit'

Chapterwise Plan

Subject Title: IC Technology

Chapter No. : 4

Chapter Name : Measurements, Packaging and Testing

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
29, 30	Semiconductor Measurements: Conductivity type, Resistivity
31,32	Hall Effect Measurements, Drift Mobility
33,34	Minority Carrier Lifetime and diffusion length
35	Packaging: Integrated circuit packages
36	Electronics package reliability
37	Testing: Technology trends affecting testing
38	VLSI testing process and test equipment, test economics and product quality

Objectives:

1. Provide an understanding of semiconductor measurements.
2. Provide knowledge about packaging and testing of Integrated circuits

Model Questions:

Q.1 Explain the concept of Hall effect measurements and drift mobility

Q.2. Explain in detail minority Carrier Lifetime and diffusion length

Chapterwise Plan

Subject Title: IC Technology

Chapter No. : 5

Chapter Name : SOI, GaAs and Bipolar Technologies

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
39	SOI Technology: SOI fabrication using SIMOX, Bonded SOI and Smart Cut
40	PD SOI and FD SOI Device structure and their features
41	GaAs Technologies: MESFET Technology
42	Digital Technologies, MMIC technologies and
43	MODFET and Optoelectronic Devices
44	Silicon Bipolar Technologies: Second order effects in bipolar transistor
45	Performance of BJT, Bipolar processes
46	BiCMOS and comparison of Technologies

Objectives:

Understand advanced semiconductor technologies

Model Questions:

Q.1. Explain in detail minority Carrier Lifetime and diffusion length

Q.2 What are MODFET and Optoelectronic Devices ?

Chapterwise Plan

Subject Title: IC Technology

Chapter No. : 6

Chapter Name : Novel Devices

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
47	Multigate Device:Various multigate device configurations
48	Device structure and important features
49	Nanowire: Fabrication and applications
50	Graphene Device:Carbon nanotube transistor fabrication, CNT applications
51	Discussion on Model questions
52	Discussion on Model questions

Objectives:

To disseminate knowledge about novel VLSI devices

Model Questions:

Q.1 State all advantages of FINFET Devices over a single gate MOSFET Device.

Q.2 Explain CNT with its advantages ,disadvantages and its applications.

Assignments

ASSIGNMENT 1 (DATE : 14th AUGUST 2015)

Q.1 Explain Float zone crystal growth process and Czochralski growth process. what is necessity of crystal growth process

Q.2. Explain the process of Bridgman growth of GaAs.

Q.3 Explain Ion implantation process in detail, also state the Gaussian expression associated with it.

Q.4.Write the kinetics of silicon growth in detail ,also state the use of high k and low k materials in semiconductor manufacturing technology.

Q.5. Draw a layout of 2 i/p CMOS NAND gate by applying appropriate ג based design rules.

ASSIGNMENT 2 (DATE : 4th October 2015)

Q.1. Explain the concept of Hall effect measurements and drift mobility

Q.2. Explain in detail minority Carrier Lifetime and diffusion length

Q.3 What are MODFET and Optoelectronic Devices ?

Q.4 Write features of SOI and MESFET Device structures

Q.5 State all advantages of FINFET Devices over a single gate MOSFET Device.

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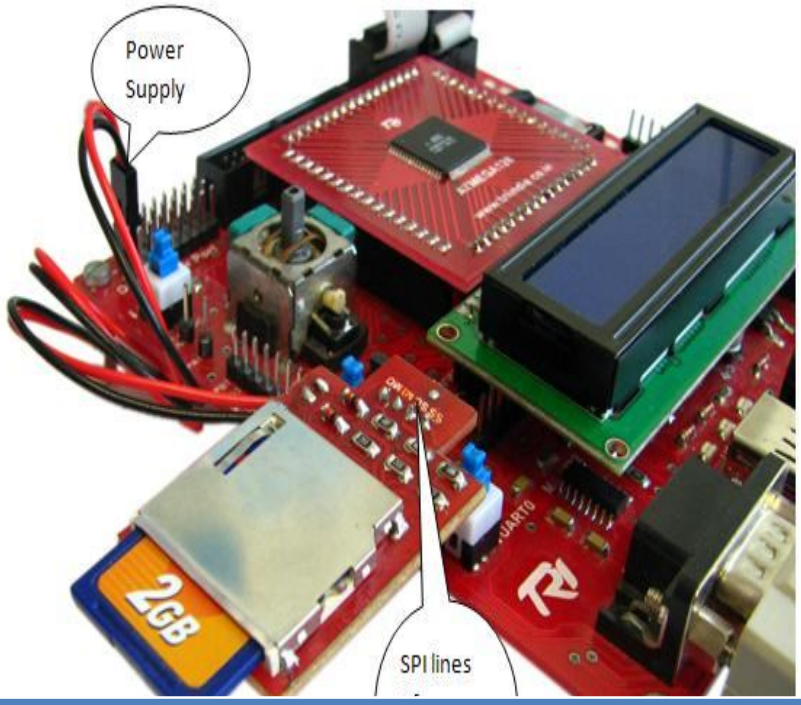

SH-2015

EMBEDDED SYSTEMS DESIGN

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
SINCERITY
SACRIFICE
SYSTEM
1990
COLLEGE OF ENGINEERING
Empower The Knowledge

Mrs.Anagha Dhavalikar

Subject Plan

DEPERTMENT : ELECTRONICS ENGINEERING
COURSE TITLE: Embedded System Design **COURSE CODE: B.E. Elex** **SEM : VII**
PRE-REQUISITE : Microprocessor and Peripherals, Microcontroller & Applications

RATIONALE

The aim of the subject is to introduce the students to the concept of Embedded Systems and their application areas. Knowledge of embedded processors like ARM, MSP 430, helps the students to use them while designing an application specific system.

OBJECTIVES:

1. To understand scope, usage, requirements, challenges and general design methodology of embedded system.
2. To thoughtfully apply hardware and software knowledge to develop embedded system applications according to requirement and constraints.
3. Apply concepts introduced in class to implement a project that utilizes embedded design methodologies and development tools.
4. Learn Real-Time hardware and software architecture and development techniques.

OUTCOME:

1. Learn to interpret design requirement; relative importance of design goals, constraints, and metric, component's functional and electrical specifications, its implication and advantage in design.
2. Select/choose right components, approach and method to develop optimal/competitive system.
3. Knowledge and understanding of fundamental embedded systems design paradigms, architectures, possibilities and challenges, both with respect to software and hardware.
4. Ability to analyze a system both as whole and in the included parts, to understand how these parts interact in the functionality and properties of the system, and properties of the system.

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes

2. Syllabus

3. Chapter wise Question Bank

Recommended Books:

1. Embedded Systems, Rajkamal , TMH, 2008.
2. Frank Vahid - Embedded Systems , Wiley India, 2002
3. ARM System-on-Chip Architecture, Steve Furber - Pearson 2005
4. Jean J Labrose - MicroC / OS-II, Indian Low Price Edition 2002
5. DR.K.V.K.K. Prasad - Embedded / real time system, Dreamtech
6. Iyer, Gupta - Embedded real systems Programming, TMH
7. Embedded systems software primer, David Simon - Pearson
8. ARM System Developers Guide- Sloss, Symes, Wright, ElsevierMorgan Kaufman, 2005
9. LPC2148 Data Sheets www.arm.com
10. ARM Programmers/architectural manual.
11. MSP430 architectural manual.
12. Embedded Microcomputer Systems – Real Time Interfacing – Jonathan W. Valvano; Cengage Learning; Third or later edition.

Internal Assessment (IA): Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the test will be considered for final internal assessment.

End Semester Examination:

1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4. Remaining question will be selected from all the modules.

List of Experiments

Suggested Laboratory Experiments:

Expt. No.	Name of the Experiments
1	Study of general hardware interfacing
2	Serial communication (between controller boards or/& any other device)
3	C-programming using GCC
4	RTOS µCOS – II IPC using message Queue
5	RTOS µCOS – II IPC using mailbox
6	RTOS µCOS – II shared resources using semaphore
7	Emulation hardware using ICE, using Logic Analyser, JTAG
8	Embedded Router Development / study
9	Embedded System Design (Theoretical design)

Chapter wise Plan

Subject Title: Embedded System Design

Chapter No. : 1

Chapter Name : Embedded System in general

Approximate Time Needed : 8 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Core of the embedded system (ASIC, SoC, GPP, DSP, IP Core)
2	Memory, Sensors/input devices (resistive, optical, position, thermal, acceleration/gravity, touch-screen), Actuators/output devices (solenoid valves, relay/switch, opto-couplers, 16x2 alphanumeric display)
3	Communication Interface, Embedded firmware (Boot-loader, RTOS, Drivers, Application programs), Power-supply (Battery technology, Solar), PWM generation, Supervisory Circuits (Watchdog, reset), PCB and Passive components. Safety, reliability, environmental, EM-radiation issues.
4	Characteristics, quality attributes and optimization challenges of Design Metric in embedded system.
5	Real time system's requirements, real time issues.
6	Hard/soft real-time systems interrupt latency.
7	Embedded Product development life cycle, Program modelling concepts: DFG
8	State machine programming models (FSM, Petri-net), Modelling for multi-processor systems, UML.

Objectives: To teach students :-

1. Different cores in embedded system
2. Types of embedded memories and various other interfaces.

Outcomes: students will learn:-

1. What do we mean by embedded systems.
2. Various embedded cores and memories

Model Questions:

No.	Questions	Year	Marks
1	Differentiate between RISC and CISC Processors.	May-2011	6
		Dec-2012	5
2	Write a note on Watchdog timer.	May-2011	5
3	Explain the interface of Alphanumeric LCD with any micro controller of your choice. (Draw neat diagram).	May-2011	7
4	What is interrupt latency in Embedded systems? Suggest methods to reduce latency.	May-2011	10
5	Explain what the Linear sequential model in Embedded software development is.	May-2011	10
6	Explain the various program modelling techniques used in embedded system design.	May-2011	10
7	Explain different types of Embedded memories.	May-2011 Dec-2011	5
8	What is H/W and S/W co-design?	May-2012	5
9	Draw and explain Petrinet model.	May-2012	3
10	Explain System on Chip (SOC).	May-2012	5
11	Explain with suitable example the following challenges met by an Embedded System Designer: I) Execution Performance II) Power Consumption III) Time to Market IV) Memory space V) Debugability VI) Cost	Dec-2012	12
12	Explain classification of Embedded system with suitable examples.	Dec-2012	8
13	Discuss design metric issues faced while designing an embedded system with the help of an example.	May-2013	5
14	Discuss and compare various embedded micro controller cores like	May-2013	5

	RISC, CISC, SOC, ARM.		
15	Differentiate between RISC and CISC processor.	Dec-2013	5
16	What is H/W and S/W co-design?	Dec-2013	5
17	with the help of suitable diagram explain: i) LCD interface ii) Hex keypad interface.	May-2014	10
18	Discuss design metric issues in designing an embedded system. Give suitable example.	May-2014	5

Chapterwise Plan

Subject Title: Embedded System Design

Chapter No. : 2

Chapter Name : Embedded Serial Communication

Approximate Time Needed : 4 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
9	Study of basic communication protocols like SPI, SCI
10	(RS232, RS485), I^2C, CAN,
11	Field-bus (Profibus), USB (v2.0), Bluetooth,
12	Zig-Bee, introduction to wireless sensor networks.

Objectives: To teach student:-

1. Basic communication protocols.
2. Wireless sensor networks.

Outcomes: students will learn:-

1. Basic communication protocols and their functions.

Model Questions

1	Write a note on Serial Peripheral Interface (SPI)	May-2011 Dec-2011 Dec-2012	5 5 5
2	Write short note on : Difference between RS232 and RS 485	Dec-2011 Dec-2012	5 5
3	Write a detailed note on the CAN Bus explaining its features and protocols.	May-2011 Dec-2012	7 5
4	Draw and explain data frame format of CAN bus.	May-2012	5

5	Write short note on: SPI and SCI port.	May-2012	5
6	Explain various basic serial communication methods.	May-2013	5
7	With the help of suitable block diagram explain: i) Graphic LCD ii) RS 232/485 iii) PWM DC motor (speed control) interfacing	May-2013	10
8	Give need for interprocess communication and synchronization. Describe the methods of the same (IPC) in detail.	May-2013	10
9	Give features of CAN and explain protocol.	May-2013	5
10	Draw and explain CAN bus frame format.	Dec-2013	5
11	Describe with suitable diagram, SPI interface.	Dec-2013	5
12	Discuss layered architecture of CAN node. Elaborate Transfer layer with regards to massage framing and arbitration.	May-2014	10
13	Techniques used in Interprocess Communication in Embedded System.	May-2014	5

Chapterwise Plan

Subject Title: Embedded System Design

Chapter No. : 3

Chapter Name : Embedded Hardware and Design

Approximate Time Needed : 12 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
13	Processor/Controller based case studies of: Low power hardware design(real time clock /PWM)
14	High Performance hardware design (media/entertainment), dc motor control
15	Low-cost hardware design (toy); Small and light weight design (Satellite/RC-plane controllers).
16	Introduction to ARM-v7-M (Cortex-M3)
17	Architecture, Internal organisation
18	ARM-v7-A (CortexA8)
19	Architecture, Internal organisation
20	ARM-v7-R (CortexR4)
21	Architecture, Internal organisation
22	Comparison between Cortex Processors
23	Direct digital solution using CPLD, FPGA, its advantages
24	introduction to related development methodology (vhdl, verilog)

Objectives: To teach students:-

1. Hardware design methodologies
2. Different ARM-v7-M Cortex series.
3. Direct digital solution using CPLD, FPGA, its advantages

Outcomes: student will learn:-

1. Different Processors of Cortex series.
2. vhdl, verilog

Model Questions

No.	Questions	Year	Marks
1	Explain various operating modes of ARM/ARM7 processors.	May-2011	10
		Dec-2011	10
		Dec-2012	10
2	Explain the register set of MSP-430 RISC controller (working registers, SFRs, Status registers etc.)	May-2011	10
		Dec-2012	10
3	Write a detailed note on THUMB mode of operation of ARM processor.	May-2011	10
4	Write a note on Digital Signal Controllers.	May-2011	5
		Dec-2011	5
		Dec-2012	5
5	Briefly explain Exceptions of ARM7	Dec-2011	10
6	Explain address space (Memory map) of MSP – 430.	Dec-2011	10
7	Explain basic clock model of MSP-430.	Dec-2011	10
		May-2012	10
8	Explain functions of different registers available in ARM7.	May-2012	5
9	Draw and explain status register structure of MSP 430.	May-2012	5
10	Explain different Exceptions which occur in MSP - 430	May-2012	5
11	Explain Processor modes of ARM7, also specify different branch instruction used to exchange branch from ARM mode to THUMB mode.	May-2012	10
12	Explain different addressing modes of ARM7TDMI.	May-2012	10
13	Draw MSP 430 architecture and write its specifications.	Dec-2012	5
14	Explain why ARM processor is one of the most commonly used 32 bit embedded processor. Draw architecture of ARM7 TDMI processor.	Dec-2012	10
15	Describe addressing modes of MSP 430 or ARM7TDMI.	May-2013	5

16	Describe the operating modes and basic clock modules of MSP 430.	May-2013	10
17	Provide description of exceptions in ARM7TDMI (interrupts).	May-2013	10
18	Explain THUMB mode ofARM7TDMI core and compare it with normal mode.	May-2013	10
19	Explain status register of MSP 430.	Dec-2013	5
20	Explain operating modes of ARM 7 and also explain Registers available in each mode.	Dec-2013	10
21	Explain clock circuit and registers used to control function of clock module of MSP 430.	Dec-2013	10
22	Compare and explain ARM7 with ARM7TDMI.	Dec-2013	10
23	Explain Interrupt Latency with example and what are the factors responsible for Interrupt Latency?	Dec-2013	5
24	Explain SPI protocol for serial communication.	May-2014	5
25	Explain clock circuit and registers used to control function of clock module of MSP 430.	May-2014	10
26	Stock implementation in ARM7. --2	May-2014	5

Chapterwise Plan

Subject Title: Embedded System Design

Chapter No. : 4

Chapter Name : Embedded Software, Firmware Concepts and Design

Approximate Time Needed : 16 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
25	Embedded C-programming concepts (from embedded system and real-time requirement's perspective): Optimizing for Speed/Memory needs, Interrupt service routines, macros, functions, modifiers, data types,
26	Device drivers, Multithreading programming. C-statements using switch, while and its ARM-assembly language equivalents. P and V semaphore functions in C.
27	Basic embedded C programs/applications for ARM-v7, using ARM-GCC-tool-chain, Emulation of ARM-v7 (e.g. using QEMU), and Linux porting on ARM-v7 (emulation) board.
28	Porting of RTOS on ARM-v7 (emulation) board, Application developments using µCOS-II.
29	Real time operating system: POSIX Compliance
30	Need of RTOS in Embedded system software
31	Foreground/Background systems, multitasking
32	context switching, IPC, Scheduler policies
33	Architecture of kernel, task scheduler
34	ISR, Semaphores, mailbox, message queues
35	pipes, events, timers, memory management
36	RTOS services in contrast with traditional OS
37	Introduction to µCOS-II RTOS, study of kernel structure of µCOS-II,

	Synchronization in µCOS-II
38	Inter-task communication in µCOS-II, Memory management in µCOS-II
39	Introduction Linux OS (Android as an example), Linux IPC usage
40	Basic Linux device drivers and its usage

Objectives: To teach students:-

1. Embedded C-programming concepts
2. Different elements in C.

Outcomes: student will learn:-

1. How to write a program in embedded C.

Model Questions

No.	Questions	Year	Marks
1	Differentiate between Object Oriented and Procedure language	Dec-2011	5
2	Suggest various techniques used for interprocess communication in an embedded system with relevant examples. Also explain strategies used for synchronization between processes.	May-2011	15
3	With the help of a neat diagram, explain the different states a task can be in and the transitions between them.	May-2011	5
4	Explain Data Structures, Queue, Circular Queue, Linked List, Array.	May-2012	10
5	Explain task and task states.	Dec-2011	5
6	Discuss various types of Semaphore in detail.	Dec-2011	10
7	Explain in detail Mutex, Pipes, Queues and Mailboxes.	Dec-2011	10
8	Write short note on: Interposes communication.	Dec-2011 Dec-2012	5 5
9	Name different problems of using Semaphore also explain priority inversion problem and its solution.	May-2012	10
10	Compare schedulers used in hard real time systems.	Dec-2012	10

11	What is shared data problem? Explain different types of semaphores.	Dec-2012	10
12	Write short notes on: Different states of tasks.	Dec-2012	5
13	With the help of suitable examples, describe following C-program elements i) Header File ii) Pre-processor Directives iii) Macro functions iv) Modifiers v) Link-List	May-2013	10
14	Describe embedded programming tools like compiler, cross complier, integrated development environment, debugging tools in circuit emulator	May-2013	5
15	Differentiate between procedures and object oriented language.	Dec-2013	5
16	Explain Data Structure Queue, Circular Queue, Link list and Array with respect to Embedded C Programming.	Dec-2013	10
17	Justify use of C programming for embedded software development.	May-2014	5
18	Explain data structure queue, circular queue, Link list and array in embedded system.	May-2014	10
19	Write ARM assembly language program to implement $\sum_{l+1}^{N} flXl \; for \; l = 1 \; to N$	May-2014	10
20	Describe embedded programming tools like compiler, cross complier, integrated development environment, in circuit emulator.	May-2014	10

Chapterwise Plan

Subject Title: Embedded System Design

Chapter No. : 5

Chapter Name : Simulation, Testing and Debugging methodology and tools

Approximate Time Needed : 4 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
41	GNU Debugger (gdb), Boundary-Scan
42	JTAG interface concepts.
43	Black-box, White-box testing
44	Hardware emulation, logic analyzer

Objectives: To teach students:-

1 Boundary-Scan/JTAG interface

2 Black-box, White-box testing

Outcomes: student will learn:-

1. Simulation and testing
2. Different debugging tools & methodologies.

Model Questions

Note on: Black Box and White Box Testing.	Dec-2013	5

Chapterwise Plan

Subject Title: Embedded System Design

Chapter No. : 6

Chapter Name : Embedded system Designing examples

Approximate Time Needed : 8 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
45	Requirement analysis, Hardware blocks diagram, System model (like FSM, UML)
46	Software architectures (modules, drivers), and Component/hardware selection,
47	Hard real time/ Mission critical: Missile, Car cruise control,
48	medical monitoring systems, process control system (temp, pressure)
49	Soft real time: Automated vending machines,
50	Digital camera, media-player.
51	Communication: Embedded web servers, routers,
52	Wireless (sensor) networks.

Objectives: To teach students:-

1. Hardware & software architectures
2. Different case studies

Outcomes: Students will learn:-

1. To design and analyse different categories of embedded systems.

Model Question

No.	Questions	Year	Marks
1	Design a FSM (Finite State Machine) for a simple elevator control system. The building has three total floors (G+2). Each floor has a call button and there are three buttons inside the elevator to choose the desired floor, discuss the operation of the system through the FSM.	Dec-2011	10
2	Explain waterfall model of embedded software development.	Dec-2011	10
3	Write short notes on: a) Programming models b) Spiral model used in EDLC c) Black box and white box testing	 Dec-2011 May-2012 Dec-2011 May-2012	 5 5 5 5
4	Design an automatic Tea and Coffee vending machine based on FSM (Finite State Machine) Model for the following requirement the tea/coffee vending is initiated by the user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin.	May-2012	7
5	Explain various programming modelling techniques used in Embedded system design.	Dec-2012	10
6	Design a car control embedded system with following specifications/features: i) It is an electric car. ii) Steering angle, acceleration, direction (R/F) are inputs from driver. Iii) It control speed, left/right steering, forward/backward direction iv) Displays speed For designing above system give 1) Show block diagram for hardware 2) Software modules/drivers diagram, flowchart	May-2013	20

	3) FSM/Petrinet model of the system. 4) Real time challenges and solutions. 5) Suggest hardware and software solutions/tools used. 6) Suggest testing, debugging, realtime issues.		
7	For an embedded system, prepaid electricity meter , whose units (readings) are down loaded wirelessly. Also a parallel LCD of a meter is installed in the house. Discuss the necessary hardware required with justification. Support your answer with suitable block diagram of the embedded electricity meter.	Dec-2013	12
8	Design an automatic tea and coffee vending machine based on FSM model for the following requirement. The tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin.	Dec-2013	8
9	Design an embedded system to measure frequency of a power line. Suggest hardware components used. Also give software architecture for the system.	May-2014	10
10	Note on: Petrinet modelling	May-2014	5
11	Note on: Waterfall model in embedded Software Development	May-2014	5

Assignment 1

1. Explain the various program modelling techniques used in embedded system design.
   with the help of suitable diagram explain: i) LCD interface ii) Hex keypad interface.
2. Give features of CAN and explain protocol.
3. Draw MSP 430 architecture and write its specifications.

Assignment 2

1. Explain in detail Mutex, Pipes, Queues and Mailboxes.
2. Note on: Black Box and White Box Testing.
3. Design an automatic tea and coffee vending machine based on FSM model for the following requirement. The tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin.

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SH-2015

COMPUTER COMMUNICATION & NETWORK

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
SINCERITY SACRIFICE
SYSTEM
1990
COLLEGE OF ENGINEERING
Empower The Knowledge

Mrs.Khushboo Singh

Subject Plan

GROUP NAME : Computer Network
COURSE TITLE : Computer Communication & Network **COURSE CODE : EXC 704** **SEM : VII (SH 2015)**
PRE-REQUISITE : Fundamentals of Communication Engineering & Digital Communication

RATIONALE

In this course students learn the fundamentals of communication networks particularly computer networks. The main purpose of this course is to introduce students with hardware requirements with its specification for the design of computer networks. This course aims to introduce the various types of data communication networks, network models, comparison of OSI model & TCP/IP model. It covers the Physical layer services & system, data link layer protocols, Network Layer services & protocols & reliable and unreliable transmission at transport layer. This course make student able to understand different types of network applications and its principle.

OBJECTIVES :

To ensure that students have the necessary networking skills to design, implement and analyze communication networks.

To describe characteristics, topologies and types of LAN technologies with appropriate reasons for the selection of LAN technology and to introduce various switching methods and analyze various routing algorithms.

To compare and contrast various digital carrier systems and to teach analysis, flow control and error control algorithms at data link layer.

To describe characteristics, topologies and types of LAN technologies with appropriate reasons for

the selection of LAN technology and to introduce various switching methods and analyze various routing algorithms.

To compare and contrast OSI model with TCP/IP stack with IP addressing and related protocols.

OUTCOME :

5. Understand the fundamentals of communication and Computer networks.
6. Have the capability of designing and analyzing data transmission protocols and data link control protocols.
7. Able to discuss major trends in industry and current research activities within the discipline.
8. Able to implement networking protocols using TCP/IP based on socket programming**.**

LEARNING RESOURCES: -

RECOMMENDED BOOKS: -

5. B. A. Forouzan, "Data Communications and Networking", TMH, Fourth Edition.
6. S. Tanenbaum, "Computer Networks", Pearson Education, Fourth Edition.
7. **Computer Networking: A Top-Down Approach, by J. F. Kurose and K. W. Ross, Addison Wesley, 5th Edition, March 2009, ISBN-13: 978-0136079675.**

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapterwise Question Bank

Evaluation :

Theory Exam	80 M
Internal assessment:-. The average marks of Mid-term test (20 M) & End-term test (20 M) will be considered as final IA marks	20 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

Atleast 10 experiments based on the entire syllabus

Expt. No.	Name of the Experiments
1	Study of network hardware & network software
2	Study of network command in Linux OS
3	Telnet services
4	SSH services
5	Bit & byte stuffing in HDLC frame format
6	Study of MODEM standards
7	Study serial communication using null modem
8	Analyze tcp traffic using opnet it guru
9	Packet analyzer using wireshark
10	Study of Wireless network

Chapterwise Plan

Subject Title: Computer Communication & Network

Chapter No. : 1

Chapter Name : Introduction to Network Architectures, Protocol Layers, and Service models

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Network Hardware: Topologies, LAN, MAN, WAN
2	Wireless network, Home Network, Internetworks, Virtual LANs
3	Network Software: Protocol Hierarchies, Design Issues for the layers
4	Connection-oriented and connectionless Services
5	Reference Models: Layers details of OSI
6	OSI Reference model
7	TCP/IP Models
8	TCP/IP Models
9	Protocol Layers
10	Their Service Models

Objectives:

1. Become familiar with the Network Hardware & software.
2. Learn the Connection oriented & Connectionless services.
3. Understand the layered task (OSI Reference Model & TCP/IP Model)
4. Know the Protocol Layers & their service models

Model Questions:

1. Compare & contrast the OSI reference model & TCP/IP Model.
2. Explain OSI Reference Model architecture for a network with two intermediate nodes, with a neat diagram. Also explain the functions of each layer. Name the layers responsible for (i) end to end reliability & (ii) link to link reliability.
3. Illustrate Connection-oriented & Connectionless Services.
4. Define network. Briefly explain the network hardware.
5. Write short notes on: Wireless network,
   Home Network,
   Internetworks,
   Virtual LANs

Chapterwise Plan

Subject Title: Computer Communication & Network

Chapter No. : 2

Chapter Name : Physical-layer Services and Systems

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Introduction to physical media, Coax, fiber, twisted pair, DSL, HFC
2	Data link layer services and protocols**:** Link-layer and its services
3	Ethernet, hubs, bridges, and switches, Link- layer addressing
4	Error-detection and error-correction. Parity, check-summing, CRC, Manchester encoding.
5	Aloha protocols, Control Access Protocol, Carrier Sense
6	Local Area Networks - Ethernet, Token ring, FDDI.
7	WiMax, cellular, satellite, and telephone networks, Bit transmission
8	FDM & TDM

Objectives:

1. Learn the various physical media.
2. Explore the data link layer services.
3. Analyze the error detection & error correction technique at data link layer
4. Understand and classify different LAN technology and application protocols.

Model Questions:

1. Explain the functions of each of these interconnecting devices: Hubs, Repeaters, Switches, Bridges, Routers & Gateways.
2. Write short notes on: Ethernet
   Token ring
   FDDI
   WiMax cellular, satellite, and telephone networks
   FDM & TDM
3. What are transmission impairments? Explain, compare co-axial cable, optical fiber cable with respect to transmission characteristic, data rate & bandwidth, application.
4. What is Ethernet? Explain fast Ethernet specifications. Also explain CSMA-CD, CSMA/CA in detail.
5. What is DSL technology? Explain various DSL technologies & compare.
6. Explain various LAN topologies.

Chapterwise Plan

Subject Title: Computer Communication & Network

Chapter No. : 3

Chapter Name : Data Link Layer Protocol

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	PPP
2	PPP
3	PPP
4	HDLC
5	HDLC
6	HDLC
7	Stop and Wait Protocol
8	Stop and Wait Protocol
9	Stop and Wait Protocol
10	Stop and Wait Protocol

Objectives:

1. Learn & explore the various data link layer protocols.

Model Questions:

1. What is data transparency? Explain the property of data transparency with reference to HDLC.
2. Explain the HDLC frame format. Describe configuration & response modes supported by HDLC protocol. Differentiate between HDLC & PPP protocols.
3. Write short notes: PPP
   Stop and wait protocols.

Chapterwise Plan

Subject Title: Computer Communication & Network

Chapter No. : 4

Chapter Name : Network layer services & protocols

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Switching fabric, Routing and forwarding
2	Queues and buffering
3	Virtual circuit & datagram network
4	Internet protocol
5	IPv4 and IPv6
6	Tunneling, LS and DV algorithms
7	Routing in the Internet, RIP
8	OSPF, and BGP
9	Broadcast and multicast
10	Handling mobility

Objectives:

1. Comprehend types of switching networks and contrast different switching methods.
2. Know the Network Protocol Layers & their services.
3. Develop and write programs for routing.

Model Questions:

1. What are the different routing protocols? Explain them briefly.
2. Compare IPv4 & IPv6.
3. Write short notes on: RIP
   OSPF
   BGP
   Broadcast and multicast

Chapterwise Plan

Subject Title: Computer Communication & Network

Chapter No. : 5

Chapter Name : Reliable and Unreliable Transport-layer Protocols

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	GBN and SR
2	TCP and UDP
3	Port numbers, Multiplexing and de-multiplexing
4	Flow control and congestion control.
5	Flow control and congestion control.
6	Fairness, Delay, jitter
7	loss in packet-switched networks
8	Bandwidth, throughput, and quality-of-service

Objectives:

1. Learn the multiplexing technique & transport layer protocols.
2. Understand the Flow control and congestion control mechanism.
3. Know the performance parameters of the packet switched network.

Model Questions:

1. Explain the performance parameters of the packet switched network.
2. What are the various flow control & error control mechanism. Explain them.
3. Write short notes on: TCP
   UDP
   GBN
   SR

Chapterwise Plan

Subject Title: Computer Communication & Network

Chapter No. : 6

Chapter Name : Principles of Network Applications

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Application layer protocols : HTTP
2	FTP, SMTP
3	Peer-to-Peer File Sharing Protocols and Architectures
4	ISPs and Domain name systems
5	Socket API
6	Network socket programming

Objectives:

1. Describe the application layer protocols.
2. Learn the Socket API & its programming.

Model Questions:

1. Illustrate Socket API
2. Define Peer-to-Peer File Sharing Protocols. Explain its architecture.
3. Write short notes on: FTP
   HTTP
   SMTP

Assignments

ASSIGNMENT 1 (DATE : 04th AUG 2015)

1. Explain OSI Reference Model architecture for a network with two intermediate nodes, with a neat diagram. Also explain the functions of each layer. Name the layers responsible for (i) end to end reliability & (ii) link to link reliability.
2. Compare & contrast the OSI reference model & TCP/IP Model.
3. Explain the functions of each of these interconnecting devices: Hubs, Repeaters, Switches, Bridges, Routers & Gateways.
4. What are transmission impairments? Explain, compare co-axial cable, optical fiber cable with respect to transmission characteristic, data rate & bandwidth, application.
5. What is Ethernet? Explain fast Ethernet specifications. Also explain CSMA-CD, CSMA/CA in detail.
6. What is DSL technology? Explain various DSL technologies & compare.

ASSIGNMENT 2 (DATE : 4th SEPTEMBER 2015)

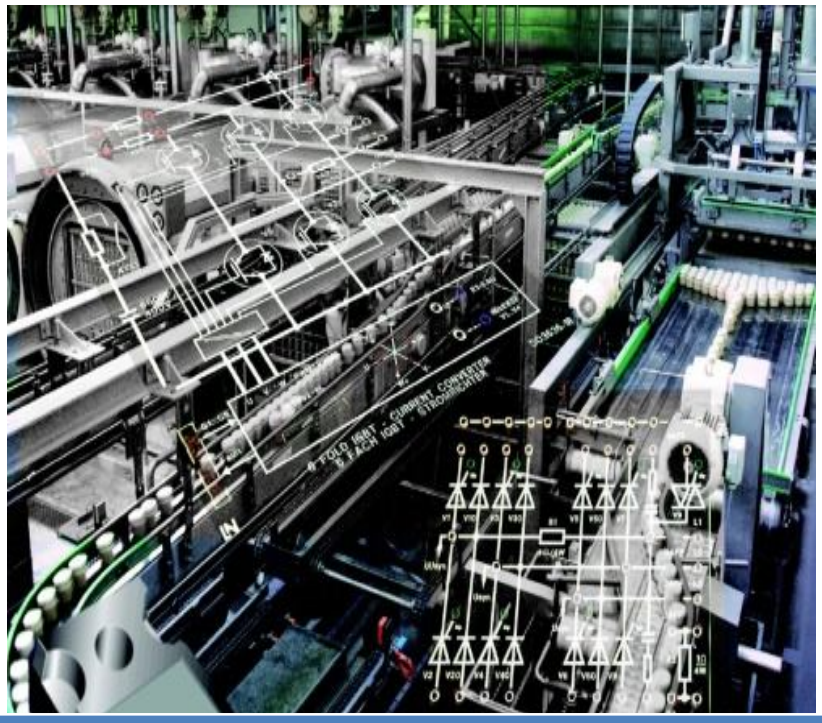
1. What is data transparency? Explain the property of data transparency with reference to HDLC.
2. Explain the HDLC frame format. Describe configuration & response modes supported by HDLC protocol. Differentiate between HDLC & PPP protocols.
3. What are the different routing protocols? Explain them briefly.
4. Compare IPv4 & IPv6.
5. Write short notes on: RIP
   OSPF
   BGP

ASSIGNMENT 3 (DATE :5th OCTOBER 2015)

1. Explain the performance parameters of the packet switched network.
2. What are the various flow control & error control mechanism. Explain them.
3. Write short notes on: TCP
   UDP
   GBN
   SR
4. Illustrate Socket API
5. Define Peer-to-Peer File Sharing Protocols. Explain its architecture.
6. Write short notes on: FTP,HTTP,SMTP

PVPP'S

College Of Engineering



SH-2015

POWER ELECTRONICS-II

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
SINCERITY SACRIFICE
SYSTEM 1990
COLLEGE OF ENGINEERING
Empower The Knowledge

Mr. Vaibhav Patil

Subject Plan

GROUP NAME: Power Electronics
COURSE TITLE: Power Electronics-II **COURSE CODE: EXC703** **SEM : VII (SH 2015)**
PRE-REQUISITE: Electronic Devices, Digital electronics

OBJECTIVES:

11. To differentiate between signal level semiconductor devices and power level semiconductor devices.
12. To teach the basic concepts of power electronics. Also to study the important power devices in detail along with basic application of controlled rectifier. To get skill of developing and design related to power electronics circuits.
13. To study the ratings of different power level semiconductor devices, its cooling techniques, and applications based on the same.
14. To study different types of converters, its working and applications.
15. To get an idea about battery charging, SMPS and UPS circuitry design.
16. To introduce different types of chopper, Inverters and their applications

OUTCOME:

1. The Knowledge of single and three phase power electronic systems.
2. Basic concepts of power electronics system design, analysis, and their application.
3. Thoroughly understand the new concepts of switching and control the power electronic system.
4. The power electronics system analysis, synthesis and their simulation.

LEARNING RESOURCES: -

RECOMMENDED BOOKS:-

1. Ned Mohan: Power electronics; John Wiley Pub.
2. M.H. Rashid, Power electronics, PHI India
3. M.D. Singh and K.B. Khanchandani. Power electronics, Tata McGraw Hill

4. J P Agrawal, Power Electronics Theory, Pearson
5. Dr. P.S. Bimbhra, Power Electroics, Khanna Publications.
6. R W Erikson: Power Electronics ; Springer
7. S Bacha, I Munteanu, A Bratcu: Power Electronics Converters, Springer
8. H Sira-Ramirez, R Silva-Ortigoza: Control systems techniques in Power electronics devices; Springer

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapter wise Question Bank

Evaluation :

Theory Exam	80 M
Internal assessment:-. The average marks of Mid-term test (20 M) & End-term test (20 M) will be considered as final IA marks	20 M
Total	100 M

List of Experiments

At least 10 experiments based on the entire syllabus

Expt.No.	Name of the Experiments
1	Simulation of single phase converters with R and RL load (With and witho freewheeling diode).
2	Simulation of Three phase converter with R and RL load.
3	Simulation of single phase, three phase converter with effect of source inductance
4	Simulation of single phase PWM Inverter
5	Simulation of Single phase and Three Phase inverter
6	Simulation of chopper with closed loop control
7	Simulation of chopper with open loop control
8	Simulation of open-loop V/f speed control of three phase induction motor
9	Simulation of open loop speed control of DC motor
10	Study of SMPS or UPS
11	To study the speed control of DC motor
12	To study the speed control of AC motor

Chapter wise Plan

Subject Title: Power Electronics II

Chapter No. : 1

Chapter Name : Rectifier and Inverter

Approximate Time Needed: 12hrs.

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Principle of operation of Rectifier
2	Effect of source inductance Single phase rectifier
3	Effect of source inductance three phase rectifier
4	Distortion in line current waveform
5	Voltage distortion for diode
6	Voltage distortion for SCR based rectifier
7	Principle of operation of Inverter
8	Three phase Voltage source Inverter
9	PWM for three phase inverter
10	Space vector Modulation Concept
11	SVM technique for three phase inverter
12	Hysteresis control

Objectives:

1. Basic concepts of power electronics. The important power devices in detail and difference between them.
2. Importance of rectifier and inverter as well as their detail working.
3. Different switching techniques for inverters

Model Questions:

1. Draw a waveform of single phase full rectifier with source induction.
2. What are differences between PWM and SVM inverter.
3. Explain three phase voltage source inverter using PWM technique.
4. Three phase VSI using space vector modulation control technique.

Chapter wise Plan

Subject Title: Power Electronics II

Chapter No. : 2

Chapter Name : DC-DC Converter

Approximate Time Needed: 10hrs.

Lesson Schedule :

Lecture No.	Portion covered per hour
13	Principle of DC converter
14	Average model of converters
15	Linearized and transfer function model
16	State space average Models
17	Basic models of Buck converter
18	Boost converter
19	Buck-Boost converter
20	Feedback control of these converters
21	Proportional Integral control
22	Proportional Integral and Differential control

Objectives:

1. Basics of dc-dc converters and its working, necessity of choppers.
2. Different types of dc-dc converter with various models and their application.
3. Feedback controls for close loop systems.

Model Questions:

1. Explain transfer function model of buck and boost converter.
2. State space average model of buck-boost converter.
3. Explain PI controller for feedback control of converter.
4. Explain PID controller for feedback control of converter.

Chapter wise Plan

Subject Title: : Power Electronics **II**

Chapter No. : 3

Chapter Name : Power Electronics Application

Approximate Time Needed : 06hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
23	Use of Power Electronics System
24	Switch Mode Power Supply
25	Battery charging system
26	Uninterrupted Power Supply
27	Induction Heating
28	Power system application

Objective:

1. The knowledge of power electronics in various applications.
2. Some important power electronics application SMPS, UPS, etc.
3. Induction heating circuits and to store energy from solar and wind detail study of battery charging systems

Model Questions:

1. What are converters used in SMPS? Explain push-pull converter.
2. What is induction heating? Explain in detail.
3. Types of UPS. Explain short break static ups configuration.
4. Give details of battery charging system.

Chapter wise Plan

Subject Title: Power Electronics II

Chapter No. : 4

Chapter Name : Power Electronics Application in DC drives

Approximate Time Needed: 10 hrs.

Lesson Schedule :

Lecture No.	Portion covered per hour
29	Basics of DC Motor and its types
30	Speed control in DC motor
31	Various schemes to control DC motor speed
32	Basics of single phase half wave semi converter
33	Single phase half wave semi converter for separately excited DC motor
34	Basics of single phase full converter
35	Single phase Full converter for separately excited DC motor
36	DC Motor Breaking
37	Dynamic breaking of dc motor
38	Regenerative breaking of dc motor

Objective:

1. Basics principles of DC motors and types of dc motor and working.
2. Various control systems to control dc motors
3. Details of single phase half wave and full wave converter drives for separately excited dc motor.
4. Different modes of breaking such as dynamic and regenerative.

Model Questions:

1. Explain working principle of separately excited DC motor.
2. What are the various schemes of DC motor speed control?
3. Explain dynamic & regenerative breaking of DC motor.
4. Explain single phase full converter drive for separately excited DC motor.

Chapterwise Plan

Subject Title: : Power Electronics **II**

Chapter No. : 5

Chapter Name : Power Electronics Application in AC motor

Approximate Time Needed : 14 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
39	Introduction to AC motors
40	Basic operation of AC motors
41	Various types of AC motor
42	Basic operation, working of induction motor
43	Three phase induction motor
44	Various speed control method for three phase induction motor
45	Stator voltage method
46	Variable frequency Method
47	Rotor resistance method
48	V/F (Voltage/Frequency) control method
49	Regenerative Breaking
50	Stator voltage method
51	Comparison of these methods
52	Revision

Objective:

1. Principle and working of ac motors, Types of ac motors
2. Various control system to control speed of AC motors
3. Detail of voltage/ frequency control method, Stator voltage control, regenerative breaking, etc.

Model Questions:

1. Explain the working of three phase induction motor.
2. What are the techniques of speed control of induction motor.
3. Explain stator voltage control & rotor resistance control of induction motor.
4. Details of V/F control & regenerative breaking of induction.